Lab 01: Quartus Prime Tutorial

ECE 380-002

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**Introduction**

In this lab, I have got familiar with VHDL, a hardware description language, and Quartus Prime, CAD software. I have gone through three design methods in the CAD software, Quartus.

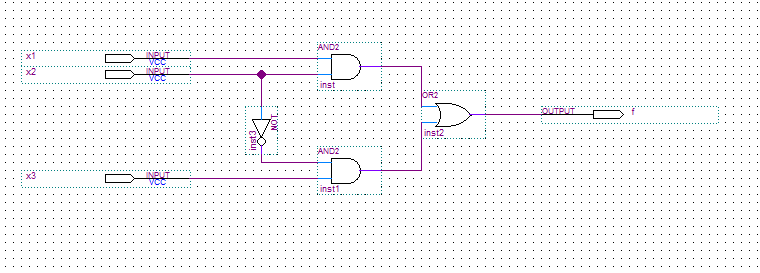
**Procedure**

1. Prelab

There was no prelab for this lab.

1. Setup and Data Collection

We followed the steps from the tutorial guide for the lab1.

Firstly, we create a new project named example\_schematic. In the project, we create the Block Diagram File called example\_schematic.bdf (Figure1). Then we compile the project and run the stimulation by creating a VWF file called A screenshot of a cell phone

Description automatically generatedexample\_schematic.vwf. (Figure2)

**0 -> 0 -> 1 -> 1**

**0 -> 1 -> 0 -> 1**

**0 -> 0 -> 1 -> 1**

**0 -> 0 -> 1 -> 1**

**Figure 1 example\_schematic.bdf**

**1**

**1**

**0**

**1**

**1**

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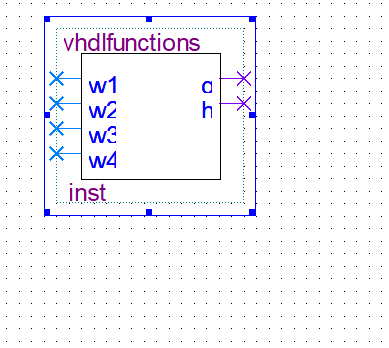
**Figure 2 example\_schematic.vwf**

A screenshot of a cell phone

Description automatically generatedSecondly, we create the second project called example\_vhdl. In this project, we create a VHDL file called example\_vhdl.vhd. (Figure3) Then, we compile the file and run the stimulation step like the first project, the file name is example\_vhdl.vwf. (Figure4)

**Figure 3 example\_vhdl.vhd**

A screenshot of a cell phone

Description automatically generatedA screenshot of a cell phone

Description automatically generatedFinally, we create the project named example\_mixed1. In the project, we create a symbol called vhdlfunctions.bsf (Figure5) by coding a VHDL file called vhdlfunctions.vhd (Figure6). Then we create a block design file called example\_mixed1.bdf (Figure7) and connect the circuits by the guide. After compiling, we A screenshot of a cell phone

Description automatically generatedcreate a file called example\_mixed1.vwf (Figure8) to simulate the circuit.

**Figure 6 vhdlfunctions.vhd**

**0**

**0**

**1**

**1**

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**0**

**1**

**0**

**1**

**0**

**0**

**0**

**0**

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**0**

**0**

**Figure 4 example\_vhdl.vwf**

**Figure 5 vhdlfunctions.bsf**

**X2: 0 -> 0 -> 1 -> 0 -> 0**

**W4: 0 -> 0 -> 1 -> 1 -> 0**

**W3: 0 -> 1 -> 1 -> 0 -> 1**

**F: 0 -> 1 -> 1 -> 0 -> 0**

**W2: 0 -> 0 -> 1 -> 1 -> 0**

**W1: 0 -> 1 -> 0 -> 0 -> 0**

**0**

**1**

**0**

**1**

**0**

**0**

**0**

**0**

**1**

**0**

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**Figure 7 example\_mixed1.bdf**

A screenshot of a social media post

Description automatically generated**Conclusion**

**Figure 8 example\_mixed1.vwf**

During the lab time, we have learned that there are three ways to construct the circuit which are schematic, VHDL and mixed. In the lab, we also get familiar with the software.

**Afterword**

Attached is a copy of the sheet used to collect information during lab, which has the verification signature on it. (Figure 9)

A close up of text on a white background

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**Figure 9 Lab Sheet**